NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

INNOVATIVE MEMORY SYSTEMS, INC.,
Appellant

v.

MICRON TECHNOLOGY, INC.,
Appellee

2018-1348

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2016-00320.

Decided: September 18, 2019

EDWARD C. FLYNN, Eckert Seamans Cherin & Mellott, LLC, Pittsburgh, PA, argued for appellant. Also represented by PHILIP LEVY; ROBERT WILLIAM MORRIS, White Plains, NY.

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Before PROST, *Chief Judge,* REYNA and STOLL, *Circuit Judges.*

REYNA, *Circuit Judge.*

Innovative Memory Systems, Inc. appeals a decision of the Patent Trial and Appeal Board in an *inter partes* review proceeding determining that claims 8–10 of the challenged patent were unpatentable as obvious. Because the Board did not err in concluding that the challenged claims are unpatentable, we affirm.

BACKGROUND

I.

Innovative Memory Systems, Inc. ("IMS") owns U.S. Patent No. 6,169,503 ("the '503 patent"). The '503 patent relates generally to digital-to-analog converters ("DACs") and analog-to-digital converters ("ADCs") that use conversion arrays containing non-volatile memory cells. '503 patent, Abstract. The '503 patent involves the use of a conversion array comprised of a plurality of transistors (also referred to as reference or memory cells) with threshold voltages that conduct in response to a digital or analog input signal. *Id.* col. 2 ll. 34–50. The conversion array may include read only memory cells that set the cells' threshold voltages or programmable non-volatile memory cells. *Id.* col. 2 ll. 60–66. The conversion array may consist of multiple rows and columns of memory cells. *Id.* col. 3. ll. 14–16.

Claims 8 and 9 are at issue in this appeal and relate to ADCs:

> 8. A converter comprising:
>
> an array of reference cells, the reference cells having a plurality of threshold voltages;
>
> a sense circuit coupled to the array; and

an encoder coupled to the sense circuit, wherein the encoder generates a multi-bit digital output signal that represents a value that depends on which of the reference cells conduct when an analog input signal is applied to a set of reference cells, wherein the encoder comprises a counter coupled to count pulses from the sense circuit, the multi-bit digital output signal being a count of the number of reference calls [*sic*] that conduct.

9. A converter comprising:

an array of reference cells, the reference cells having a plurality of threshold voltages, wherein the array contains a plurality of rows;

a sense circuit coupled to the array; and

an encoder coupled to the sense circuit, wherein the encoder generates a multi-bit digital output signal that represents a value that depends on which of the reference cells conduct when an analog input signal is applied to a set of reference cells; and

a row decoder coupled to the array, the row decoder selecting a row of reference cells to which the analog signal is applied.

Id. col. 12 ll. 20–47.

II.

Micron Technology, Inc. ("Micron") filed a petition for *inter partes* review of claims 1 and 8–10 of the '503 patent. The Patent Trial and Appeal Board ("Board") instituted review on all challenged claims and grounds. In its initial Final Written Decision, the Board found that Micron had shown by a preponderance of the evidence that claim 8 was obvious based on the combination of U.S. Patent No. 5,376,935 ("Seligson") and U.S. Patent No. 4,591,825

("Bucklen"), or Seligson, U.S. Patent No. 5,187,483 ("Yonemaru"), and Bucklen. The Board also found that Micron had shown that claims 9 and 10 were obvious based on the combination of Seligson and Yonemaru.[1] At the same time, the Board denied a motion filed by IMS to exclude portions of a declaration submitted by Micron's expert, Dr. Baker ("the Baker Reply Declaration"), in support of Micron's reply brief.

IMS then filed a request for rehearing, which the Board granted. The Board withdrew its initial Final Written Decision and authorized IMS to file a sur-reply to respond to Micron's reply brief. After IMS filed its sur-reply, the Board issued its Final Written Decision After Rehearing, maintaining its determination that claims 8, 9, and 10 were unpatentable and its denial of IMS's motion to exclude. J.A. 74.

The Board's conclusion that claim 8 was obvious depended on its construction of the recited "counter" term. The Board construed the claim term "counter . . . to count pulses" to mean an "accumulator, circuit, or device that calculates the number of pulses" according to the plain meaning of its words under the broadest reasonable interpretation standard. J.A. 22–29. The Board rejected IMS's contention that "[o]ne of ordinary skill in the art would understand that a 'counter' is something that uses *sequential* logic to count *individual pulses*, not a transition detection circuit that uses combinational logic to locate the transition point from which the ultimate count may be determined." J.A. 22–23 (quoting Patent Owner's Response) (emphasis added by Board). The Board considered the language of the claim and the specification and determined

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[1] During the course of proceedings, IMS disclaimed claim 1 of the '503 patent, so it was not part of the Final Written Decision.

that claim 8 does not require the counter to count each sensed pulse individually as IMS argued. *See* J.A. 23–25.

To ascertain the plain meaning of "counter," the Board considered extrinsic evidence, including expert testimony and dictionaries. The Board found that the record evidence supported that the plain meaning of "counter . . . to count pulses" means an "accumulator, circuit, or device that calculates the number of pulses." J.A. 26. After considering whether the specification deviated from this plain meaning, the Board determined that the specification did not clearly limit the claimed "counter" to a sequential counter and instead contemplated counters more broadly. J.A. 26–28. Based on its resolution of the claim construction dispute over the "counter" phrase and IMS's concession that Bucklen disclosed such a device, the Board concluded that claim 8 was obvious. *See* J.A. 56–58, 62.

As noted above, the Board also determined that the combination of Seligson and Yonemaru rendered claims 9 and 10 obvious.[2] J.A. 54. The Board found that claim 9 was obvious under its adopted construction of "the row decoder selecting a row of reference cells to which the analog signal is applied" to mean "the row decoder selecting one or more rows of reference cells to receive the analog input signal, or selecting one or more rows that already have the analog signal." J.A. 22, 38. The Board also found that even under IMS's narrower proposed claim construction, which "require[d] the row decoder [to] select a row of reference cells to receive the analog input signal," the combination of Seligson and Yonemaru rendered claims 9 and 10 obvious. J.A. 38.

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[2] IMS did not present any arguments individually directed to claim 10 before the Board and does not do so on appeal.

The Board found that "Seligson's transistors include reference voltages and inputs, which function similarly to the reference resistors and inputs in Yonemaru, and Yonemaru discloses select switches ultimately to provide different selected rows of voltage references for comparisons." J.A. 38–39. It further found that "modifying Yonemaru's decoder and select switches to select at least one row of programmable reference transistors in Seligson's circuit to attach an input voltage to a row would have been obvious for the purpose of sensing different analog ranges, while providing a known array configuration for utilizing available chip space." *Id.*; *see also* J.A. 40 ("Seligson and Yonemaru would have suggested employing Yonemaru's decoder to control switches SW (via signals SE) to connect an input voltage to a selected row of reference cells and thereby satisfy Patent Owner's narrower claim construction."). Relying on Micron's expert Dr. Baker's testimony, the Board rejected IMS's arguments that a person of ordinary skill in the art would lack motivation to combine Seligson and Yonemaru. *See* J.A. 40–54.

IMS appeals. We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

DISCUSSION

The Board's ultimate claim construction is a question of law that we review de novo; we review its underlying factual findings for substantial evidence. *Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1341 (Fed. Cir. 2018). In IPR proceedings, claims in an unexpired patent are given their broadest reasonable interpretation in light of the specification.[3] *Cuozzo Speed Techs.,*

[3] Despite the U.S. Patent and Trademark Office's change to the claim construction standard, the broadest reasonable interpretation standard applies in this case because the petition was filed before November 13, 2018. *See*

LLC v. Lee, 136 S. Ct. 2131, 2146 (2016). Accordingly, the words of the claim are construed according to their plain meaning, unless such a meaning conflicts with the specification or prosecution history. *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016).

Obviousness is a question of law with underlying factual findings. *Hamilton Beach Brands, Inc. v. f'real Foods, LLC*, 908 F.3d 1328, 1341 (Fed. Cir. 2018). We review the ultimate obviousness determination de novo and underlying factual findings for substantial evidence. *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). Underlying factual findings include the scope and content of the prior art and whether a person of ordinary skill in the art would have been motivated to combine references. *Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1051 (Fed. Cir. 2016). "Substantial evidence . . . means such relevant evidence as a reasonable mind might accept as adequate to support a conclusion." *Consol. Edison Co. of N.Y. v. N.L.R.B.*, 305 U.S. 197, 229 (1938).

I.

With respect to claim 8, IMS asserts that the Board's construction of "counter . . . to count pulses" as "accumulator, circuit, or device that calculates the number of pulses" was unreasonable in light of the specification. According to IMS, the broadest reasonable interpretation of the "counter" term is "a sequential circuit that goes through a prescribed sequence of states upon the application of input pulses from the sense circuit." Appellant Br. 24. We disagree.

Beginning with the language of the claim, "a counter coupled to count pulses from the sense circuit" does not

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Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018).

require a counter that counts pulses in any particular way. '503 patent col. 12 ll. 30–31. Turning to the written description, there is no dispute that it does not "clearly set forth a definition" of "counter," and the patentee has not "act[ed] as [his] own lexicographer" here. *Bradium Techs. LLC v. Iancu*, 923 F.3d 1032, 1044 (Fed. Cir. 2019) (quoting *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)).

IMS points to an embodiment in the specification disclosing a sequential counter as depicted in Figure 5B. Yet it is well established that "it is not enough for a patentee to simply disclose a single embodiment or use a word in the same manner in all embodiments, the patentee must 'clearly express an intent' to redefine the term." *Id.*; *Acumed LLC v. Stryker Corp.*, 483 F.3d 800, 805 (Fed. Cir. 2007) ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments." (quoting *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005))). The patentee expressed no such clear intent here.

Further, in the embodiment relied on by IMS, the patentee specified that the counter counts sequentially from zero. *See* '503 patent col. 6 ll. 12–15 ("Counter 532 provides the address signal to select circuits 524 in bias and sense circuits. For signal conversion, a clock signal causes counter 532 to sequentially count up from zero."). This suggests that the broader meaning of the term as used in the patent encompasses a wider scope of counters. *See Acumed*, 483 F.3d at 809 (declining to construe "transverse holes" as limited to perpendicular holes despite every description in the patent contemplating a perpendicular hole).

Thus, the Board did not err in rejecting IMS's narrower proposed construction. Further, the Board properly relied on extrinsic evidence to confirm that the broadest reasonable interpretation of the term "counter" tracks the plain

meaning of the claim language. We discern no error in the Board's construction of "counter . . . to count pulses" as "accumulator, circuit, or device that calculates the number of pulses." There is no dispute that Bucklen discloses a "counter" and that the Board properly found there was sufficient motivation to combine the references under this construction. We therefore affirm the Board's determination that Micron showed by a preponderance of the evidence that claim 8 is obvious in view of Seligson and Bucklen, or Seligson, Yonemaru, and Bucklen.

II.

With respect to claim 9, IMS asserts that the combination of Seligson and Yonemaru does not render the claim obvious under the proper construction of "row decoder selecting a row of reference cells to which the analog signal is applied." IMS argues that the "row decoder" must "select a row of reference cells to receive the analog input signal, not a row of reference cells to which the analog input signal is already being applied." Appellant Br. 46. Relying on a hand-drawn figure that Dr. Baker drew during his deposition, IMS asserts that Dr. Baker conceded that the combination circuitry of Seligson and Yonemaru would determine the output of the transistors, where "the analog input signal was applied to all rows at the same time." Appellant Br. 52. According to IMS, this combination fails to satisfy the limitations of claim 9.

As noted above, the Board made alternative factual findings that the combination of Seligson and Yonemaru discloses the "row decoder" limitation under IMS's narrower construction of the term and that a person of ordinary skill in the art would have been motivated to combine the references. We therefore do not address IMS's claim construction arguments because substantial evidence supports these alternative findings.

As a preliminary matter, the teachings of the prior art are not limited by what Dr. Baker's deposition drawing

purportedly shows, and the Board correctly observed that Dr. Baker was not required to sketch out all the circuit details of the combination of Seligson and Yonemaru to provide sufficient evidence of obviousness. *See* J.A. 53 (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981) ("The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.").

The Board cited to Figure 4 of Seligson, which discloses a circuit diagram of an ADC circuit with a plurality of electrically programmable transistors with reference voltages coupled to an analog voltage input IN_A. J.A. 38; *see also* Seligson Fig. 4, col. 7 ll. 16–34. The Board also cited to Figure 1 of Yonemaru, which discloses a similar ADC circuit with reference resistors and inputs and switches for selectively applying voltage references for comparison. J.A. 38; *see also* Yonemaru Fig. 1, col. 5 l. 52–col. 6 l. 35. The Board further cited to the Baker Reply Declaration, explaining Dr. Baker's view that the row decoder disclosed by Yonemaru "connects a respective row to the analog-to-digital path" and Seligson's disclosure of the row of "reference cells that accept the analog signal on their gates" such that they together disclose the "row decoder" limitation, which "could include selecting only one row" to which the analog signal could be applied and is consistent with IMS's construction. J.A. 1839–40 (Baker Reply Decl.). Citing to the Petition and Yonemaru, the Board explained how it would be obvious for the purpose of sensing different analog ranges to modify Yonemaru's decoder and "SW switches" to select one or more rows of reference transistors in the Seligson circuit to connect the input voltage. J.A. 38–39. The Board also found that Yonemaru teaches using "switches SW to select input reference voltages" to

compare the input reference voltages to the analog input signal "thereby effectively switching compared input . . . values into the encoder to create digital outputs." J.A. 40 (citing Yonemaru Fig. 1, Abstract, col. 6 ll. 11–49). Dr. Baker also opined that adding a switch would be easy to do for someone wanting to connect the analog input signal to one row. J.A. 42 (citing J.A. 3142 (Baker Dep. Tr.)).

The Board further credited Dr. Baker's testimony that his modification of using switches to connect a row of reference cells would involve additional transistors but would generally reduce the overall footprint compared to a long single row. J.A. 41 (citing J.A. 1846–47 (Baker Reply. Decl.)). It further credited Dr. Baker's testimony that a person of ordinary skill would have been motivated to combine Seligson and Yonemaru such that the analog signal was applied to as few transistors and rows as possible (e.g., one row) to reduce load and power requirements and increase speed. J.A. 42 (citing J.A. 1847–48 (Baker Reply Decl.)).

In summary, the Board analyzed the references, made detailed fact findings regarding their disclosures and the motivation of a person of ordinary skill to combine them, including specific citations to the references and the record, and addressed, in detail, the expert testimony. The bulk of IMS's arguments are disagreements with the Board's factual findings and expert credibility determinations, which warrant our deference. *E.g., Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) ("We defer to the Board's findings concerning the credibility of expert witnesses."). Thus, we discern no error in the Board's determination that claims 9 and 10 are unpatentable as obvious under IMS's narrower proposed construction.

III.

We briefly address IMS's procedural arguments regarding the Board's reliance on the Baker Reply Declaration. IMS argues that the Board erred by relying on the

Baker Reply Declaration in its Final Written Decision After Rehearing. Appellant Br. 52–56. IMS's argument is based on its assertion that the Baker Reply Declaration was improper rebuttal because it purportedly expanded on what Dr. Baker stated in his original declaration. Despite disagreeing with IMS that the Baker Reply Declaration was improper rebuttal, the Board granted IMS's request for rehearing, withdrew its initial Final Written Decision, and gave IMS leave to file a sur-reply, even though IMS did not request further briefing or the opportunity to submit additional evidence. J.A. 66. IMS also did not request the opportunity to provide an expert declaration or additional pages of briefing after the Board granted the sur-reply. Additionally, the Board credited IMS's arguments as being endorsed by its expert, declining to dismiss any arguments as mere attorney argument. We do not determine whether the Baker Reply Declaration exceeded the scope of proper rebuttal, because even if it did, the sur-reply afforded IMS sufficient additional opportunity to be heard. Accordingly, the Board did not abuse its discretion in denying IMS's motion to exclude portions of the Baker Reply Declaration.

CONCLUSION

We have considered IMS's remaining arguments and find them unpersuasive. For the foregoing reasons, we affirm the Board's decision.

AFFIRMED

COSTS

Each party shall bear its own costs.