NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

INNOVATIVE MEMORY SYSTEMS, INC.,
Appellant

v.

MICRON TECHNOLOGY, INC.,
Appellee

2017-2472

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2016-00330.

Decided: August 27, 2019

EDWARD C. FLYNN, Eckert Seamans Cherin & Mellott, LLC, Pittsburgh, PA, argued for appellant. Also represented by PHILIP LEVY; ROBERT WILLIAM MORRIS, White Plains, NY.

JARED BOBROW, Orrick, Herrington & Sutcliffe LLP, Menlo Park, CA, argued for appellee. Also represented by JEREMY JASON LANG; DOUGLAS WAYNE MCCLELLAN, Weil, Gotshal & Manges LLP, Houston, TX.

Before PROST, *Chief Judge*, REYNA and STOLL, *Circuit Judges*.

PROST, *Chief Judge*.

Innovative Memory Systems, Inc. ("IMS") appeals from the final written decision of the Patent Trial and Appeal Board ("Board") in an inter partes review filed by Micron Technology, Inc. ("Micron"). The Board concluded that the challenged claims of U.S. Patent No. 6,901,498 ("the '498 patent") were unpatentable in view of the prior art of record. For the reasons below, we affirm-in-part, reverse-in-part, vacate-in-part, and remand.

I

The '498 patent generally relates to non-volatile memory. A non-volatile memory, such as a flash memory, can be "divided into logical zones" in order to "reduce the size of the data structures it uses for address translation." '498 patent col. 6 ll. 25–28. The '498 patent involves "methods to adjust the zone boundaries to accommodate defects allowed by memory test to improve card yields and to adjust boundaries in the field to extend the usable lifetime of the card." *Id.* col. 6 ll. 29–32. Independent claim 1 is representative and recites:

> 1. A memory system circuit, comprising:
>
> a memory comprising a plurality of blocks of non-volatile storage elements wherein the storage elements within individual ones of the blocks are simultaneously erasable, and
>
> a controller that controls programming of data into addressed blocks, reading data from addressed blocks and erasing data from one or more of addressed blocks at a time, wherein the memory is organized into logical zones each comprised of one or more blocks for address translation, and wherein

> the correspondence of blocks to zones is adjustable by controller.

Id. col. 12 ll. 56–67.

In December 2015, Micron filed an IPR challenging claims 1, 2, 5, 6, 11, 12, 15, 16, 21, 22, 27, 32, 33, 38, 43, 44, 47, and 48 of the '498 patent. The Board instituted review on four grounds: (1) claims 1, 2, 11, 12, 21, 27, 32, 38, 43, and 44 are unpatentable as obvious over European Patent No. 0 896 280 A2 ("Tanaka") in view of U.S. Patent No. 6,034,897 ("Estakhri"); (2) claims 5, 6, 15, 16, 47, and 48 are unpatentable as obvious over Tanaka in view of Estakhri and U.S. Patent No. 7,020,739 ("Mukaida"); (3) claims 5, 6, 15, 16, 47, and 48 are unpatentable as obvious over Tanaka in view of Estakhri and U.S. Patent No. 6,088,264 ("Hazen"); and (4) claims 22 and 33 are unpatentable as obvious over Tanaka in view of Estakhri and U.S. Patent No. 6,260,156 ("Garvin"). *Micron Tech., Inc. v. Innovative Memory Sys., Inc.*, No. IPR2016-00330, Paper 10 at 27 (P.T.A.B. June 29, 2016) ("*Institution Decision*").

After an oral hearing, the Board determined that Micron had demonstrated by a preponderance of the evidence that all challenged claims were unpatentable based on the asserted grounds. *Micron Tech., Inc. v. Innovative Memory Sys., Inc.*, No. IPR2016-00330, Paper 40, 2017 WL 2704099, at *18 (P.T.A.B. June 22, 2017) ("*Final Written Decision*").

IMS appealed. We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

II

"We review the Board's ultimate claim constructions de novo" and "any subsidiary factual findings involving extrinsic evidence for substantial evidence." *AC Techs. S.A. v. Amazon.com, Inc.*, 912 F.3d 1358, 1365 (Fed. Cir. 2019). A claim in an unexpired patent is given its broadest

reasonable construction.[1] *See* 37 C.F.R. § 42.100(b) (2017); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2146 (2016). Under this standard, "words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history." *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016).

Obviousness is a question of law based on underlying factual determinations. *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). We review the ultimate obviousness determination de novo and underlying factual findings for substantial evidence. *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). "A finding is supported by substantial evidence if a reasonable mind might accept the evidence to support the finding." *K/S Himpp v. Hear-Wear Techs., LLC*, 751 F.3d 1362, 1364 (Fed. Cir. 2014).

III

IMS first contends that the Board erred in determining that the combination of Tanaka and Estakhri renders obvious the claim limitation "wherein the correspondence of blocks to zones is adjustable by controller" in claim 1, and related limitations in claims 11 and 43. IMS challenges the Board's construction of the term and the Board's analysis of the prior art. We address each in turn.

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[1] The U.S. Patent and Trademark Office changed the claim construction standard used in IPR proceedings. *See* 37 C.F.R. § 42.100(b); *Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board*, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (to be codified at 37 C.F.R. pt. 42). The new standard applies only to petitions filed on or after November 13, 2018, and therefore does not impact this case.

A

IMS contends that the Board improperly construed the term "wherein the correspondence of blocks to zones is adjustable by controller." Below, IMS argued that the phrase means "adjusting zone boundaries such that blocks from one logical zone are shifted to another logical zone." *Final Written Decision* at *4. The Board rejected this requirement that the blocks being adjusted must come from an existing "logical zone." *See id.* at *5. It found that the plain and ordinary meaning "is broad enough to encompass both the situation where blocks are assigned to zones and the situation where the blocks are not yet assigned." *Id.* It did not further construe the term. On appeal, IMS argues this construction was unreasonably broad in light of the plain language of the claims and the specification. We agree.

We begin with the claim language. In claim 1, the "controller" must be able to adjust "the correspondence" between blocks and zones. Therefore, the outcome here turns on the meaning of "the correspondence." The Board concluded that the plain and ordinary meaning of "correspondence" is simply any "connection" or "relation." *Id.* But that does not end the inquiry. The claim is not written as "a correspondence." Rather, as written, the plain language of the claims requires "*the* correspondence."

The phrase "the correspondence" establishes there is a preexisting connection or relationship between the blocks and zones. The relationship is defined in the claim. Indeed, it is described in the "wherein" clause directly before the disputed limitation. In full, the two phrases together read: "wherein the memory *is organized into logical zones each comprised of one or more blocks* for address translation, and wherein *the correspondence of blocks to zones* is adjustable by controller." '498 patent col. 12 ll. 64–67 (emphases added). Claim 11 recites the same "wherein" language. *Id.* col. 13 ll. 35–39.

Read together, the two wherein clauses leave no doubt about the proper construction. Blocks are organized into zones. When blocks become defective in a zone, the claim recites a solution: "the correspondence of blocks to zones" can be adjusted. Thus, IMS's construction that "blocks from one logical zone are shifted to another logical zone" is required by the claim language.

The same holds true for claim 43. Claim 43 recites "logical address section" instead of "logical zones." But it also recites the same existing "correspondence" between "logical address sections" and "blocks." *Id.* col. 16 ll. 5–9 ("[W]herein the non-volatile [*sic*] is organized into logical address sections as seen by the controller, wherein the correspondence between physical blocks and logical address sections is adaptable by the controller in response to defects in the memory").

The specification confirms this reading of the plain language of the claims. In every embodiment disclosed in the '498 patent specification, zone boundaries are adjusted by transferring blocks from one logical zone organized for address translation to another logical zone organized for address translation. *See, e.g.*, *id.* col. 6 ll. 24–32, 40–44, col. 7 ll. 35–51, col. 8 ll. 20–34. Micron does not dispute this point. *See* Appellee's Br. 30. In light of the clear scope of the claims, which is only further supported by the specification, the Board's construction was unreasonably broad.

Resisting this conclusion, Micron makes several arguments that the claims are not limited. None are persuasive. First, it argues that IMS's construction must fail because the claims do not expressly use the term "boundaries." Appellee's Br. 27. The Board appears to have been led astray by this argument. *See Final Written Decision* at *5 ("Importantly, the identified passages of the Specification discuss adjusting zone boundaries, but the claims do not use the term 'boundaries.'"). Certainly, the claims could have been written to describe this process as

redrawing the "boundaries" between zones. But it was not necessary. Per the claim language, the blocks in question must be organized into zones. The claims recite changing the "correspondence" between the zone and its components—blocks already part of zones—to assist zones with defective blocks. Whether expressed as changing "boundaries" or adjusting "correspondence," the outcome is the same.

Next, Micron points to the Board's reasoning that claim 1 refers to several different types of "blocks." *Id.* (discussing the "plurality of blocks" that comprise the memory, "addressed blocks," and the "one or more blocks" organized into logical zones). Micron infers that since certain "blocks" (e.g., "plurality of blocks") referenced elsewhere in the claim are not expressly tied to a particular zone, the claims must encompass adjusting blocks that have no affiliation to a zone.

This misreads the claim language. If one examines the claim in full and follows the antecedent basis for each element, Micron's argument about unaddressed blocks unravels. Claim 1 requires a "memory system circuit." The circuit must have "*a memory* comprising a plurality of blocks" wherein "*the memory* is organized into logical zones each comprised of one or more blocks for address translation." In turn, "*the correspondence* of blocks to zones is adjustable by [the] controller." The claim goes from a broad category ("a memory") including the different types of memory Micron identifies, to a much more finite class of memory ("the memory" organized into logical zones of "one or more blocks for address translation"). It is this finite class of "the memory" that "the correspondence of blocks to zones" refers back to. As such, the broader list of memory at the outset of the claim has no bearing on this specific limitation.

Finally, the cases Micron cites are inapplicable here. Micron points to our decisions discussing the rigors of

proving specification disclaimer. *See, e.g.*, *Unwired Planet, LLC v. Apple Inc.*, 829 F.3d 1353, 1358 (Fed. Cir. 2016) ("We do not read this specification as clearly and unmistakably requiring that voice signals be transmitted exclusively over voice channels."). But in such cases, the issue was whether the specification disclaimed or otherwise limited the broader scope of the claim as written. By contrast, here the narrow scope is already established by the plain text of the claims itself. In other words, the specification is not being used to narrow the claim, triggering the disavowal doctrine. Rather, the specification simply supports the conclusion being drawn from the text of the claim on its face.

For the reasons above, we reverse the Board's construction for the term "wherein the correspondence of blocks to zones is adjustable by controller" in claim 1 and the related term in claims 11 and 43. The term requires that the controller can adjust zone boundaries such that blocks from one logical zone are shifted to another logical zone.

B

We now turn to the Board's analysis of the prior art. Below, the Board addressed IMS's narrower construction in the alternative. It concluded that Tanaka still discloses a controller "adjusting zone boundaries such that blocks from one logical zone are shifted to another logical zone." *See Final Written Decision* at *10. According to the Board, Tanaka discloses taking spare blocks unassociated with an address and assigning them to a zone. *Id*. The Board found that those blocks come from a "redundant block area." *Id*. In the Board's view, this area could be considered a logical zone, though none of the blocks within it are assigned to an address. *Id*. Because Tanaka discloses making zone adjustments by transferring redundant blocks from the "redundant block area" (i.e., a first logical zone) to a second area where defective blocks are located (i.e., a second logical zone), the Board found that Tanaka satisfies IMS's

construction. *Id.* (citing Subramanian Decl. ¶ 25; Subramanian Dep. 58:8–59:13). The Board's reasoning was not meaningfully different for claims 11 or 43. *See, e.g.*, *Final Written Decision* at *13 ("Our reasoning regarding why Tanaka satisfies the limitations of claims 1 and 11 also applies here to claim 43, even though claim 43 recites 'logical address sections,' instead of 'zones'; because, as discussed above, Tanaka's zones and redundant block are logical address sections within the meaning of claim 43.").

IMS argues the Board's analysis ignored the requirements of the claim. We agree. The Board cut the analysis short. The claim does not simply require that the memory is organized into "logical zones" of any nature.[2] The full claim limitation expressly requires that the memory is "organized" into "logical zones *each comprised of one or more blocks for address translation*." '498 patent col. 12 ll. 64–66 (emphasis added). Thus, the zones contain blocks that are already assigned for address translation. As discussed above, the properly construed remaining language in the claim then requires a controller that can adjust boundaries between zones of assigned blocks "such that blocks from one logical zone are shifted to another logical zone."

Based on the record, IMS insists there is no evidence supporting a finding that Tanaka meets the full limitation. It encourages us to reverse. Reversal, rather than remand, is appropriate where, "[o]n the evidence and arguments presented to the Board, there is only one possible evidence-supported finding: [that] the Board's determination . . . when the correct construction is employed, is not supported by substantial evidence." *Corning v. Fast Felt Corp.*, 873 F.3d 896, 900–01 (Fed. Cir. 2017). According to IMS, there is no evidence to show that the "redundant block area" in

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[2] The term "logical zones" was construed to mean "a logical subdivision of the total capacity of the non-volatile memory die." *Id.* at *10.

Tanaka is a zone in which memory is already organized or mapped to an address. IMS's expert, Dr. Nettles, testified that these redundant blocks do not have logical addresses until they are used to replace a defective block. J.A. 1677 (Nettles Decl. ¶¶ 105–106). Micron's expert, Dr. Subramanian, appeared not to dispute this point. J.A. 19–1920 (Subramanian Dep. 27:2–16).

We think the better course is to remand to the Board for determination of the factual issue under the proper construction. Consequently, we vacate the Board's conclusion about this limitation and remand for further proceedings regarding whether the prior art teaches this limitation in independent claims 1, 11, and 43 and their respective dependent claims (2, 5, 6, 12, 15, 16, 44, 47, and 48).

IV

Separately, IMS challenges the Board's finding that the combination of Tanaka and Estakhri discloses "a single controller" in independent claims 1, 11, 21, 32, and 43. The claims all recite a *single* controller that performs two functionalities. The first functionality requires the controller to control "programming," "reading," and "erasing" of data. *See, e.g.*, '498 patent col. 12 ll. 61–63. The second functionality is expressed slightly differently across different claims. In some claims, the controller must be able to "adjust[]," (claims 1 and 11) or "assign[]" (claims 21 and 32) blocks to zones. *Id.* col. 12 l. 67, col. 13 l. 38, col. 14 ll. 11–12, col. 14 ll. 65–66. In other claims, the controller must be able to "adapt[]" (claim 43) the blocks to "logical address sections." *Id.* col. 16 ll. 7–9.

IMS disputes that Micron proved the combination of Tanaka and Estakhri discloses "a single controller." IMS's argument on appeal boils down to two points. First, IMS seems to argue waiver. Second, it argues failure of evidence. Neither position is persuasive.

Regarding its waiver-style arguments, IMS contends that Micron never advanced a theory that it would have been obvious to put Tanaka's functionality—which involves the second functionality of zone adjustment—in Estakhri's controller. Appellant's Br. 55. According to IMS, Micron only ever argued the reverse. Contrary to IMS's position, however, Micron's petition appears to have raised the theory. According to the petition:

> [T]o the extent that Tanaka does not expressly disclose that the controller is performing the remapping (or the same controller as in claim [1.2]), it would have been obvious from Tanaka in view of Estakhri that the same "controller device 14" in Estakhri (or of Tanaka) that controls the programming (i.e., writing), reading, and erasing of data could also perform the above-mentioned zone adjustments.

J.A. 128 (Petition); *see also* J.A. 715 (Subramanian Decl.).

As for failure of proof, IMS contends that there is a lack of substantial evidence to support this theory. We disagree. Not only did Micron's petition disclose the theory of combining the redundant circuit functionality in Tanaka's system into the controller of Estakhri, but it provided substantial evidence in support of this theory, including through the declaration of Dr. Subramanian. *See, e.g.*, J.A. 708–14, 715–17, 886 (Abstract); *see also* J.A. 894 (col. 1 ll. 64–66, col. 2 ll. 20–22, col. 2 ll. 38–50), 896 (col. 5 ll. 34–36), 1589–90 (¶ 36).

Relatedly, IMS further contends that Micron neglected to offer any evidence of a motivation to combine Tanaka's functionality with Estakhri's controller. We disagree. The record here confirms Micron presented several evidentiary bases. Micron's expert, Dr. Subramanian, testified that using the controller of Estakhri in Tanaka would have involved a simple substitution that would have been

understood to yield predictable results and would have been obvious to try. *See* J.A. 683–84 (Subramanian Decl. ¶¶ 80–82). Dr. Subramanian also opined that a person of ordinary skill "would have used the controller and planes of Estakhri in the Tanaka system because both address the specific issue of logically grouping flash blocks together and erasing multiple blocks at a time." J.A. 681–83 (Subramanian Decl. ¶¶ 78–79). On this record, substantial evidence supports a finding of motivation to combine. *See* J.A. 27–28.

This was the only challenge on appeal to independent claims 21 and 32. Therefore, we affirm the Board's conclusion that claims 21 and 32 are unpatentable as obvious. Likewise, as IMS raises no other challenge to dependent claims 22, 27, and 38, we also affirm the Board's conclusions that these claims were unpatentable as obvious.

V

For the reasons above, we reverse the Board's claim construction of "wherein the correspondence of blocks to zones is adjustable by controller" and vacate and remand its obviousness determination for further analysis regarding whether claims 1, 2, 5, 6, 11, 12, 15, 16, 43, 44, 47, and 48 are unpatentable as obvious over the combination of Tanaka and Estakhri. We affirm the Board's conclusion that claims 21, 22, 27, 32, 38 are unpatentable.

AFFIRMED-IN-PART, REVERSED-IN-PART, VACATED-IN-PART, AND REMANDED

COSTS

The parties shall bear their own costs.