NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

IN RE ERIC JASINSKI, MICHAEL RICHARD OUELLETTE, AND JEREMY PAUL ROWLAND,
Appellants.

2012-1482

Appeal from the United States Patent and Trademark Office, Board of Patent Appeals and Interferences.

Decided: February 15, 2013

ANTHONY P. NG, Yufell Isidore Ng Russell, PLLC, of Austin, Texas, argued for appellants.

MONICA B. LATEEF, Associate Solicitor, Office of the Solicitor, United States Patent and Trademark, Office, of Alexandria, Virginia. With her on the brief were RAYMOND T. CHEN, Solicitor, and SCOTT C. WEIDENFELLER, Associate Solicitor

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Before PROST, CLEVENGER, and MOORE, *Circuit Judges.*

MOORE, *Circuit Judge*.

Eric Jasinski et al. appeal from the decision of the Board of Patent Appeals and Interferences (Board) affirming the examiner's rejection of all claims during prosecution of patent application number 10/906,508 ('508 application). For the reasons set forth below, we *reverse* and *remand*.

BACKGROUND

The '508 application relates to the diagnosis of memory device failures. When a memory tester detects a failure in a memory device, the logical address of the memory error must be translated into a physical address within the memory device. This translation is typically performed by logical-to-physical mapping software. The '508 application claims systems and methods for verifying the accuracy of this logical-to-physical mapping software.

The '508 application discloses a built in self-test (BIST) control function that generates "simulated" memory failures at predetermined physical locations in a memory device. A memory tester then tests the memory device and records the logical memory addresses of any locations having errors. Logical-to-physical mapping software maps the logical memory addresses to physical addresses within the memory device. Finally, to "verify the accuracy of [the] logical-to-physical mapping software," the physical addresses mapped by the logical-to-physical mapping software is compared to the predetermined or "simulated" physical addresses at which the BIST control function generated memory failures.

Claim 1 of the '508 application is representative:

> A method for *verifying the accuracy of logical-to-physical mapping software* designed for testing memory devices, said method comprising:
>
> [a] providing a built-in self test (BIST) fail control function to generate multiple simulated memory fails at various predetermined locations within a memory array of a memory device;
>
> [b] testing said memory array via a memory tester;
>
> [c] generating a bit fail map by said logical-to-physical mapping software based on all memory fails indicated by said memory tester, wherein said bit fail map indicates physical locations of all fail memory locations derived by said logical-to-physical mapping software; and
>
> [d] comparing said fail memory locations derived by said logical-to-physical mapping software to said various predetermined memory locations *to verify the accuracy of said logical-to-physical mapping software*.

'508 application claim 1 (emphases added).

The Patent and Trademark Office (PTO) rejected all claims in the '508 application as anticipated by U.S. Patent No. 5,912,901 to Adams. The Board affirmed, concluding that the language, "[to verify/verifying] the accuracy of [said] logical-to-physical mapping software," recited in the preambles and "comparing" limitations of claims 1, 9, and 17 is a statement of intended use and does not limit the claims. The Board also concluded that even if this language is limiting, Adams discloses it.

Mr. Jasinski appeals. We have jurisdiction under 28 U.S.C. § 1295(a)(4).

DISCUSSION

Anticipation is a question of fact. *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991). We uphold the Board's factual findings unless they are not supported by substantial evidence. *In re Gartside*, 203 F.3d 1305, 1316 (Fed. Cir. 2000). We review the Board's "broadest reasonable" claim interpretation *de novo*. *In re Abbott Diabetes Care Inc.*, 696 F.3d 1142, 1148 (Fed. Cir. 2012).

A.

Mr. Jasinski argues that the Board erred by failing to give "patentable weight" to the preamble language "verifying the accuracy of logical-to-physical mapping software designed for testing memory devices" in claims 1, 9, and 17. Mr. Jasinski further argues that the Board committed the same error with respect to the recitation of "to verify the accuracy of said logical-to-physical mapping software" in the comparing steps of the same claims and similar language in dependent claims 8, 16, and 24. Mr. Jasinski argues that the "to verify/verifying" language should be considered a limitation because it is "the essence of the invention."

The government responds that the "to verify/verifying" language is nothing more than a statement of intended purpose. It contends that the Board's constructions were reasonable because the claims do not inform a person of ordinary skill how the comparing or concluding steps are executed.

We agree with Mr. Jasinski. Not only does the "to verify/verifying" language refer to the "essence of the invention," it also provides the criteria by which the previously-recited comparing limitation is analyzed. We thus conclude that the "to verify/verifying" language is limiting. *See Vizio, Inc. v. Int'l Trade Comm'n*, 605 F.3d 1330, 1341 (Fed. Cir. 2010) ("[T]he 'for decoding' language . . . is properly construed as a limitation, and not merely a

statement of purpose or intended use for the invention, because 'decoding' is the essence or a fundamental characteristic of the claimed invention.").

B.

Mr. Jasinski argues that Adams does not teach verifying the accuracy of the logical-to-physical mapping software. Mr. Jasinski concedes that Adams teaches comparing the contents read from a memory device with a predetermined bit pattern that was previously written into the memory device. Mr. Jasinski argues, however, that Adams does not teach verifying the accuracy of the logical-to-physical mapping software by comparing the set of physical locations at which memory errors were detected (determined by the logical-to-physical mapping software) with the set of various predetermined physical memory locations at which the BIST routine generated errors.

The government argues that Adams discloses mapping logical addresses to physical addresses using logical-to-physical mapping software and that the output of such mapping is used in additional "failure analysis." The government argues that one of ordinary skill in the art would deduce that one of the possible failures detected by additional "failure analysis" is defective logical-to-physical mapping software.

The government, however, has failed to establish anticipation. The Adams reference does not disclose verifying the accuracy of logical-to-physical mapping software. Adams merely discloses a BIST routine for detecting errors within a memory device by comparing memory *contents* with a predetermined bit pattern. The fact that it states that the output of the mapping can be used in additional "failure analysis" is not the same thing as disclosing those additional types of failure analysis. Adams does not disclose the detection of errors in logical-to-physical mapping software by the comparing of sets of

physical memory *locations* as claimed, and thus does not anticipate. Adams nowhere indicates that "failure analysis" would include defective logical-to-physical mapping software, and it also fails to explain how that analysis would be performed. Although some of the government's arguments appear to suggest that the claims at issue may have been obvious, that issue is not before us on appeal. The only rejection made by the examiner and affirmed by the Board is anticipation by a single reference. That reference, Adams, simply does not anticipate.[1] Accordingly, the decision of the Board is

REVERSED AND REMANDED.

[1] On appeal, Mr. Jasinski also argues that Adams fails to disclose the generation of "multiple simulated memory fails at various predetermined locations" as required by the first step of claim 1. On appeal, the government contends that we ought not consider this distinction between Adams and the claims at issue because Mr. Jasinski did not raise the issue below. On remand, however, should prosecution continue, Mr. Jasinski would be free to argue this distinction.