NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

RAMBUS INC.,
Appellant,

v.

Teresa Stanek Rea, ACTING DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE,
Appellee.

2012-1480
(Reexamination No. 95/001,166)

Appeal from the United States Patent and Trademark Office, Board of Patent Appeals and Interferences.

Decided: June 28, 2013

JOHN M. WHEALAN, of Chevy Chase, Maryland, argued for appellant. Of counsel on the brief were JEFFREY A. LAMKEN and MICHAEL G. PATTILLO, JR., MoloLamken, LLP, of Washington, DC; and KARA F. STOLL, Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, of Washington, DC.

COKE M. STEWART, Associate Solicitor, Office of the Solicitor, United States Patent and Trademark Office, of Alexandria, Virginia, argued for appellee. With her on the brief were RAYMOND T. CHEN, Solicitor, NATHAN K. KELLEY, Deputy Solicitor, and WILLIAM LAMARCA, Associate Solicitor.

Before RADER, *Chief Judge,* O'MALLEY, and WALLACH, *Circuit Judges.*

Opinion for the court filed by *Chief Judge* RADER.

Dissenting opinion filed by *Circuit Judge* WALLACH.

RADER, *Chief Judge.*

This appeal arises from an *inter partes* reexamination proceeding before the United States Patent and Trademark Office (PTO). The Board of Patent Appeals and Interferences (Board) affirmed the Examiner's rejection of all 25 claims of U.S. Patent No. 7,287,109 (the '109 Patent) under 35 U.S.C. § 102(a). Because substantial evidence does not support the Board's conclusion, this court reverses.

I.

The technology at issue involves methods of controlling a dynamic random access memory device (DRAM). Storing information in a DRAM is referred to as a "write" operation, and retrieving information from a DRAM is referred to as a "read" operation. Information is written to, or read from, a DRAM using a memory controller. For example, in a write operation, a memory controller transmits control information to the DRAM, which includes a write request and "address" information indicating where (by row and column) the data will be stored. The DRAM receives the control information and executes the write operation, *i.e.*, writes the data to the corresponding location. Data and control information are trans-

ferred between the memory controller and the DRAM through a set of lines called a "bus."

Prior to 1990, DRAMs operated "asynchronously" to the memory controller—that is, read and write operations were not conducted with reference to a system clock. A DRAM would execute read/write operations *as quickly as possible* after receiving control information from the memory controller. Between the time the memory controller transmitted the control information and the time the DRAM executed the operation, the memory controller had to wait for the DRAM to complete internal preparatory functions. This interface between the memory controller and the DRAM rendered the bus unusable because it would freeze in a "wait state" where the memory controller could not perform any other functions until the read/write operation was executed.

As processor speeds increased, DRAMs could not keep up, which created a bottleneck that diminished the advantages of faster processors. The 1990s, however, introduced the synchronous DRAM, which executed read/write operations with reference to a system clock. After the memory controller transmitted a read/write request to the DRAM, the DRAM would wait a pre-determined number of clock cycles before executing the operation. This clock function eliminated the "wait state" and enabled the memory controller to perform other tasks and send additional requests to other DRAMs while the operation was pending. This process became known as "interleaving." This case features different methods of interleaving.

II.

Rambus is the owner of the '109 Patent, entitled "Method of Controlling a Memory Device Having a Memory Core." It claims priority to U.S. Patent Application No. 08/545,292, filed on October 19, 1995, by Richard M. Barth, et al. In 2009, the PTO granted NVIDIA Corporation's request for *inter partes* reexamination of

the '109 Patent. The Examiner rejected all 25 claims as anticipated by an earlier Rambus patent, U.S. Patent No. 6,584,037 (Farmwald). The Board affirmed the rejection and Rambus sought rehearing. Meanwhile, Rambus and NVIDIA settled, and NVIDIA withdrew from the proceedings. The Board denied rehearing, and Rambus appealed to this court where the sole issue on appeal is whether substantial evidence supports the Board's finding that the '109 Patent is anticipated by Farmwald.

The '109 Patent discloses and claims certain methods of controlling data transfers to and from a DRAM. As the Board found, the specification describes "at least two embodiments," which the Board referred to as the "strobe" embodiment and the "non-strobe" embodiment. J.A. 3; *see* '109 Patent col. 10 ll. 25–67. In both embodiments, a memory controller transmits a request packet to the DRAM. '109 Patent col. 10 ll. 25–67. The request packet contains control information indicating whether the DRAM will perform a read or a write operation. J.A. 3–4.

In the strobe embodiment, the memory controller then transmits a separate "strobe signal" to the DRAM, which causes the DRAM to execute the operation immediately (with a minimal inherent delay). J.A. 4; '109 Patent col. 8 l. 63–col. 9 l. 7; '109 Patent col. 9 ll. 41–46. As the Board noted, the benefit of this invention "stems from latency minimization, resulting in a relatively free data bus for other data transfers—i.e., the command control information tells the [DRAM] to pre-fetch the desired data . . . and the [DRAM] then waits for the strobe signal to send the data." J.A. 4.

In the non-strobe embodiment, the memory controller "varies the timing of data transmission without use of the above-described strobe signal." J.A. 5. Rather, "the [request] packet contains a delay value that indicates to the DRAM when the [operation should be executed] relative to the time at which the request packet is sent."

J.A. 4–5 (quoting '109 Patent col. 10 ll. 52–60). For example, if the request packet contained a write request and a delay value of eight clock cycles, the DRAM would execute the write operation after eight clock cycles elapse. As the Board noted, the benefit here is that the "[memory] controller is able to *dynamically* adjust the operative interleave." J.A. 6 (emphasis added).

III.

The Farmwald patent, titled "Memory Device which Samples Data after an Amount of Time Transpires," likewise discloses and claims a method of controlling data transfers to and from a DRAM. As the Board found, Farmwald teaches using a memory controller to send a request packet to the DRAM, which contains control information specifying a read or write operation. J.A. 8. Farmwald's request packet also contains a bit that selects an "access-time register" within the DRAM. J.A. 8; Farmwald col. 9 l. 54–col. 10 l. 1. The access-time registers are central to Farmwald's invention.

Each of Farmwald's DRAMs contains "access-time registers 173 which store a set of one or more delay times at which the device can or should be available to send or receive data." Farmwald col. 6 ll. 40–45. For example, one access-time register might contain a delay value of two system clock cycles, another four system clock cycles, and another eight, and so forth. The access-time registers "can be modified and preferably are set as part of an initialization sequence that occurs when the system is powered up or reset." Farmwald col. 6 ll. 45–47. In other words, the delay values are stored in the access-time registers on start-up, prior to the memory controller transmitting any request packets to the DRAM. J.A. 10993 ("Farmwald relies upon the previously received [delay] value signal . . . .").

As the Board found, Farmwald teaches that after the memory controller transmits a request packet to the

DRAM, the DRAM will wait to execute the specified read/write operation depending on which access-time register is selected by the bit in the request packet. J.A. 8; Farmwald col. 9 ll. 23–25 ("The time after which a data block is driven onto the bus lines is selected from values stored in slave access-time registers."). For example, if the request packet contains a bit that selects access-time register no. 4, and access-time register no. 4 was previously programmed with a delay value of eight clock cycles, the DRAM will execute the operation contained in the request packet after eight clock cycles elapse.

IV.

The '109 Patent and Farmwald are no strangers to one another. First, the '109 Patent specification distinguishes Farmwald as prior art. For example, the '109 Patent describes Farmwald's method of controlling a DRAM as "inflexible" because the start of an operation is tied to "a predetermined number of clock cycles" after the request packet is transmitted, and "the number of clock cycles . . . may be determined by a value stored in a register within the DRAM." '109 Patent col. 10 ll. 32–37.

Moreover, Farmwald's parent patent, U.S. Patent No. 5,319,755 (Farmwald '755), shares the same specification as Farmwald and was cited by the Examiner during initial examination of the '109 Patent application. The Examiner rejected the '109 Patent claims as being anticipated by Farmwald '755, but withdrew the objection after Rambus responded to the Office Action.

Further, the '109 Patent has been widely litigated in at least seven causes of action. In at least two of these actions, Farmwald or Farmwald '755 were directly in front of the tribunal. In ITC Investigation No. 337-TA-661, the Respondents and Staff Attorney advanced similar arguments as the Board does in the present case, but the Commission affirmed the ALJ's conclusion that Farmwald '755 does not anticipate the '109 Patent.

Certain Semiconductor Chips Having Synchronous Dynamic Random Access Memory and Prods. Containing Same, Inv. No. 337-TA-661, 2011 WL 6016982 (October 1, 2011). Likewise, in ITC Investigation No. 337-TA-753, the ALJ held in an Initial Determination that Farmwald does not anticipate the '109 Patent. Certain Semiconductor Chips and Prods. Containing Same, Inv. No. 337-TA-753, 2012 WL 927056 (March 2, 2012).

Notwithstanding the above, the Board found in the present case that Farmwald anticipates the '109 Patent. In other words, a reference that was overcome during initial examination, distinguished as prior art in the patent specification, and found not to anticipate by at least two different tribunals, now—according to the Board—discloses each and every element of the claims. The result is somewhat surprising, especially with nothing in the record indicating whether the Board considered these prior decisions. Upon comparison of the relevant claims, this court concludes that Farmwald does not anticipate the '109 Patent's claims.

V.

This court reviews the Board's factual findings for substantial evidence. *In re Gartside*, 203 F.3d 1305, 1316 (Fed. Cir. 2000). Anticipation is a question of fact. *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991). "A claim is anticipated only if each and every element as set forth in the claim is found . . . in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). This court reviews the Board's claim construction de novo. *Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1456 (Fed. Cir. 1998) (en banc).

The parties agree that claim 1 is representative of all claims:

> 1. A method of controlling a memory device having a memory core, wherein the method comprises:
>
> Providing control information to the memory device, wherein the control information includes a first code which specifies that a write operation be initiated in the memory device;
>
> Providing a signal to the memory device, wherein the signal indicates when the memory device is to begin sampling write data, wherein the write data is stored in the memory core during the write operation;
>
> Providing a first bit of the write data to the memory device during an even phase of a clock signal; and
>
> Providing a second bit of the write data to the memory device during an odd phase of the clock signal.

'109 Patent col. 41 l. 61–col. 43 l. 2. The central issue is whether Farmwald discloses the step of "providing a signal to the memory device, wherein the signal indicates when the memory device is to begin sampling write data."

The Board construed the term "signal" broadly to mean "the physical representation of data," and concluded that Farmwald discloses such a signal. The Board's construction of the term "signal" is unreasonably overbroad. Indeed, construing the term "signal" to mean any representation of data would essentially convert every element of claim 1 into a signal because the control information, including the write command and the data being written, are all physical representations of data.

The patent specification makes clear that "signal" is being used in a narrower sense as a start indicator for the DRAM to begin an operation. *See, e.g.*, '109 Patent Ab-

stract ("A signal is provided that indicates when the memory device is to begin sampling write data . . . .").

This court does not need to re-construe the term "signal," however. Nor does this court need to reach the question of whether "signal" encompasses just the "strobe signal" in the strobe embodiment of the '109 Patent, or whether it also encompasses the delay value in the non-strobe embodiment. Even under the Board's broad construction, Farmwald does not anticipate the '109 Patent's claims.

The Board held that Farmwald's method of storing and recalling delay values from the DRAM's access-time registers anticipated the "providing a signal" limitation of claim 1 in one of four ways. The Board stated, "Farmwald's delay value . . . is either "1) in the request packet; 2) stored in an access-[time register]; 3) provided for comparison to a clock; and/or 4) implicitly used to generate another implicit signal after comparison to signify a match." J.A. 13. These theories are discussed in turn below. The court notes that the Board's failure to pick one theory of anticipation it found persuasive, or even most persuasive, itself causes questions about the Board's confidence in its anticipation rejection.

1. In the Request Packet

The Board stated that Farmwald's delay value is "in the request packet" transmitted from the memory controller to the DRAM. J.A. 13. The record does not support this view. The record shows that Farmwald's delay value is previously stored in an access-time register within the DRAM. Farmwald col. 6 ll. 40–47; J.A. 10993 ("Farmwald relies upon the previously received [delay] value signal . . . ."). Although Farmwald's request packets contain a bit that selects an access-time register, this feature differs from claim 1, which requires "a signal . . . [that] indicates when the memory device is to begin sampling write data." '109 Patent cl. 1. The bit in Farmwald's

request packet does not contain any timing information, but merely selects an access-time register. Although subsequent events or signals from the access-time registers may cause the DRAM to begin an operation, that part of the Farmwald operation does not transform the bit into a signal that meets the limitations of the claim. The invention claimed in the '109 Patent eliminates the need for access-time registers—a significant advantage over the prior art. '109 Patent col. 10 ll. 27–39.

2. Stored in an Access-Time Register

The Board alternatively held that "storing the delay value in the access-time register" in Farmwald anticipates the "providing a signal" step of claim 1. J.A. 14. However, Farmwald's delay values are stored in the access-time registers prior to the memory controller transmitting any request packets to the DRAM. Thus, the Board's interpretation requires performance of the first two steps of claim 1 out of order. While the steps of a method are not limited to a specific order unless the claim explicitly or implicitly so requires, *Baldwin Graphics Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1345 (Fed. Cir. 2008), here, a plain reading of claim 1 evinces a specific order. The first step of claim 1 "specifies that a write operation be initiated in the memory device," and the second step "indicates when the memory device is to begin sampling write data." '109 Patent cl. 1. It would make no sense for the second step to be performed first—telling the memory device to begin sampling write data—before the memory device was even instructed to perform a "write" operation. Therefore, the Board's finding is clearly erroneous.

The Board also stated that "skilled artisans would have considered . . . *retrieving* [the delay value]" from Farmwald's access-time register as constituting "providing a signal." J.A. 14 (emphasis added). The record also supplies no support for this finding. Farmwald's access-time registers are within the DRAM, and thus, the DRAM

is essentially "retrieving" the delay value from itself. Claim 1 of the '109 Patent requires "[p]roviding a signal *to* the memory device." '109 Patent cl. 1 (emphasis added). The Board's reasoning that "[c]laim 1 does not preclude providing the signal from one part of the memory device to another part of it," J.A. 15 n.3, can neither be reconciled with the plain language of the claim nor the patent specification, which is replete with references and figures showing an external memory controller transmitting signals to the DRAM. *See*, *e.g.*, '109 Patent col. 4 ll. 8–26.

3. Provided for Comparison to a Clock

The Board stated that "skilled artisans would have considered . . . comparing [Farmwald's delay value] to a clock value . . . as also constituting 'providing a signal,' as recited in claim 1." J.A. 14. However, nowhere did the Board identify where Farmwald discloses this comparison; nor did the Board explain how "comparing" a delay value to a clock value equates to a "signal," particularly under the Board's construction of "signal" to mean "the physical representation of data." This court has made clear that "[b]road conclusory statements standing alone are not evidence." *In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000). In this case, the Board does not show that comparing a delay value to a clock signal anticipates the claim.

4. Implicitly Used to Generate Another Implicit Signal After Comparison to Signify a Match

The Board again, without any discussion or citation to Farmwald, determined that "Farmwald's system implicitly compares a clock signal to [the] register-stored delay value, and thereafter implicitly generates another signal for completing the data read or write operation upon a determination that the clock counter equals the delay value. . . ." J.A. 12. The record does not support this finding. Furthermore, the implicit signal relied on by the Board appears to be generated from the access-time

registers. As mentioned above, Farmwald's access-time registers are located within the DRAM itself, and claim 1 of the '109 Patent requires a signal be provided to the DRAM from an external source. Therefore, even assuming that Farmwald's system implicitly generates a signal upon determination that the clock counter equals a delay value, the signal would not anticipate the claim.

VI.

In conclusion, the Board's determination that all 25 claims of the '109 Patent are invalid as anticipated by Farmwald is not supported by substantial evidence. Accordingly, this court reverses.

REVERSED

United States Court of Appeals for the Federal Circuit

RAMBUS INC.,
Appellant,

v.

Teresa Stanek Rea, ACTING DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE,
Appellee.

2012-1480
(Reexamination No. 95/001,166)

Appeal from the United States Patent and Trademark Office, Board of Patent Appeals and Interferences.

WALLACH, *Circuit Judge*, dissenting.

The Board's conclusion that the patent is anticipated is supported by substantial evidence, and therefore I dissent from the majority's decision.

The dispositive question in this case is whether substantial evidence supports the Board's finding that Farmwald discloses the step of "providing a signal to the memory device, wherein the signal indicates when the memory device is to begin sampling write data. . . ." '109 patent col. 42 ll. 61–63. It is uncontested that Farmwald's DRAM contains "access-time registers" with various delay values. Farmwald teaches sending a "request packet" from a memory controller to the DRAM with control

information that, *inter alia*, selects an access-time register. The Board found that this request packet was a "signal" that "indicates" when the DRAM "is to begin sampling write data." This is supported by substantial evidence. Although the delay value choices are stored in the DRAM, a reasonable person could conclude that the request packet is a "signal" that "indicates" when the DRAM "is to begin sampling write data." *Id.* col. 42 ll. 61-63; *see Consol. Edison Co. v. Nat'l Labor Relations Bd.*, 305 U.S. 197, 229 (1938) (Substantial evidence "means such relevant evidence as a reasonable mind might accept as adequate to support a conclusion."); *In re Kotzab*, 217 F.3d 1365, 1369 (Fed. Cir. 2000) ("Substantial evidence is something less than the weight of the evidence but more than a mere scintilla of evidence.").

The majority says that although Farmwald's request packets contain a bit, that bit merely selects an access-time register; it does not contain any timing information itself. However, given the Board's broad construction of the term "signal," which the majority accepts, *see* Maj. Op. 9, the bit in the request packet provides a signal by selecting an access-time register which indicates when the DRAM is to begin an operation. It is the bit that selects an access-time register, and therefore indicates "when the memory device is to begin sampling write data." '109 patent col. 42 ll. 62–63. That is, the request packet includes a bit, a "value," that tells the memory device to wait x amount of time after receiving the command to write data. The fact that the x is stored within the memory device does not change what the value represents. Without the value in the request packet the memory device would not know when to begin sampling; it is that bit which instructs the memory device when to begin. Farmwald teaches that the request packet controls the timing of writing data either by directly "select[ing] a certain register in the slave DRAM memory device which stores the (delay value) timing information" or indirectly

by "indicat[ing] pre-selected (delay value) access times." *See* J.A. 8 (citing Farmwald col. 9 l. 46 – col. 10 l. 5)). Contrary to the majority's characterization, no subsequent steps or signals are necessary. *See* Maj. Op. 8–9. Once the specified amount of time elapses, sampling begins. Farmwald col. 27 ll. 19–20 (Claim 25 specifies "outputting the data to the memory device after a delay time transpires.").

The second basis for the Board's reasoning is that the claim language does not require sequential reading of the first two steps. The first two steps state:

> Providing control information to the memory device, wherein the control information includes a first code which specifies that a write operation be initiated in the memory device;
>
> Providing a signal to the memory device, wherein the signal indicates when the memory device is to begin sampling write data, wherein the write data is stored in the memory core during the write operation . . . .

'109 patent col. 41 l. 64 – col. 42 l. 64. The "write operation" instruction does not need to come before the claimed "signal" since that signal only indicates when the "write operation" is to happen. There is no reason the write instruction and the signal indicating the timing of the write operation could not come at the same time—like they do in Farmwald's request packet.

The majority states that "a plain reading of claim 1 evinces a specific order," because "[i]t would make no sense for the second step to be performed first—telling the memory device to begin sampling write data—before the memory device was even instructed to perform a 'write' operation." Maj. Op. 10. However, it is not clear, as a matter of "logic or grammar," that all of the steps in claim 1 must be performed in the order written. *See Altiris, Inc.*

v. Symantec Corp., 318 F.3d 1363, 1369–71 (Fed. Cir. 2003). "[A]lthough a method claim necessarily recites the steps of the method in a particular order, as a general rule the claim is not limited to performance of the steps in the order recited, unless the claim explicitly or implicitly requires a specific order." *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1345 (Fed. Cir. 2008). The third step, "providing a first bit of the write data to the memory device during an even phase of a clock signal," and the fourth step, "providing a second bit of the write data to the memory device during an odd phase of the clock signal," have parallel structure and sequential language. '109 patent col. 42 ll. 66–67; col. 43 ll. 1–2. But the same cannot be said for the first two steps of claim 1. The first step describes a "first code" but the claim fails to identify a "second code." There is no sequential language in the first two steps to indicate that they must occur in the order written. The broadest reasonable interpretation of signal indicates *when* the operation is to happen, but does not necessarily require immediate initiation. Therefore, in instances like the '109 patent's delay value embodiment, wherein the signal instructs the DRAM to wait some number of clock cycles before initiating action, it does not matter whether the DRAM has been instructed to do a write operation until the specified period of time elapses.

The role of this court is not to determine if the record could support a different outcome, but to determine if the Board's findings are supported by substantial evidence. *In re Jolley*, 308 F.3d 1317, 1320 (Fed. Cir. 2002) (If "the evidence in [the] record will support several reasonable but contradictory conclusions," then this court "will not find the Board's decision unsupported by substantial evidence simply because the Board chose one conclusion over another plausible alternative."). Because the Board's findings on anticipation are supported by substantial evidence, I respectfully dissent.