NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

COMPUTER CACHE COHERENCY CORPORATION,
Plaintiff-Appellant,

v.

INTEL CORPORATION,
Defendant-Appellee.

COMPUTER CACHE COHERENCY CORPORATION,
Plaintiff-Appellant,

v.

VIA TECHNOLOGIES, INC. AND VIA TECHNOLOGIES, INC. (USA),
Defendants-Appellees.

2010-1040, -1041

Appeals from the United States District Court for the Northern District of California in case nos. 05-CV-1766 and 05-CV-1668, Senior Judge Ronald M. Whyte.

Decided: September 22, 2010

LAWRENCE M. HADLEY, Hennigan, Bennett & Dorman LLP, of Los Angeles, California, argued for plaintiff-appellant. With him on the brief were MIEKE K. MALMBERG and OMER SALIK.

LAUREN B. FLETCHER, Wilmer Cutler Pickering Hale and Dorr LLP, of Boston, Massachusetts, argued for defendant-appellee Intel Corporation. With her on the brief were WILLIAM F. LEE; and ARTHUR W. COVIELLO. Of counsel on the brief were TINA M. CHAPPELL, Intel Corporation, of Chandler, Arizona; KARL J. KRAMER, Morrison & Forrester, of Palo Alto, California; and HECTOR G. GALLEGOS, Morris & Forrester, of Los Angeles, California.

JULIE M. HOLLOWAY, Wilson Sonsini Goodrich & Rosati, of Palo Alto, California, argued for defendants-appellees Via Technologies, Inc., et al. With her on the brief was MONICA MUCCHETTI ENO.

Before RADER, *Chief Judge*, and LOURIE and BRYSON, *Circuit Judges*.

RADER, *Chief Judge*.

The United States District Court for the Northern District of California granted Intel Corporation's ("Intel"), Via Technologies, Inc.'s and Via Technologies, Inc. (USA)'s (collectively, "Via") motions for summary judgment of non-infringement of Computer Cache Coherency Corporation's ("CCCC") U.S. Patent No. 5,072,369 ("the '369 patent"). *Computer Cache Coherency Corp. v. Via Techs., Inc.*, Nos. 05-1668, 05-1766, 2008 WL 4368770, at *21 (N.D. Cal. Sept. 23, 2008). Because the accused products do not

include the "SNOOP signal telling" limitation, this court affirms.

I

The '369 patent, entitled "Interface Between Buses Attached Modules Interface Between Providing Address Space Mapped Cache Coherent Memory Access with Snoop Hit Memory Updates," issued on December 10, 1991, based on an April 7, 1989 application. The '369 patent claims an interface circuit that permits a first bus master connected to a first bus to access directly a main memory connected to a second bus while maintaining coherency between corresponding data in the main memory and cache memory used by a second bus master on the second bus. Claim 1 of the '369 patent, the only claim at issue on appeal, recites:

> An apparatus for providing data communication between first and second buses,
>
> the first bus providing a first plurality of bus masters connected thereto with data read and write access to first data storage locations mapped to separate addresses within a first address space, wherein one of said first plurality of bus masters writes data to a first particular one of said first data storage locations by placing on the first bus an address to which the first particular one of said first data storage locations is mapped and transmitting the data via said first bus, and wherein one of said first plurality of bus masters reads data from a second particular one of said first data storage locations by placing on the first bus an address to which the second particular one of said first storage locations is mapped and receiving data via said first bus,

the second bus providing a second plurality of bus masters connected thereto with data read and write access to second data storage locations mapped to separate addresses within a second address space, wherein one of said second plurality of bus masters writes data to a first particular one of said second data storage locations by placing on the second bus an address to which the first particular one of said second data storage locations is mapped and transmitting the data via said second bus, and wherein one of said second plurality of bus masters reads data from a second particular one of said second data storage locations by placing on the second bus an address to which the second particular one of said second storage locations is mapped and receiving data via said second bus,

wherein one of said second plurality of bus masters connected to said second bus caches data read out of a subset of said second data storage locations, said second bus including means for conveying a SNOOP signal with an address appearing on the bus, *the SNOOP signal telling said one of said second plurality of bus masters when to write cached data to the address appearing on the bus*,

the apparatus comprising:

first mapping means coupled to said first bus for mapping first addresses within the first address space to second addresses within the second address space, for asserting an indicating signal and for generating one of said second addresses in response to one of said first addresses transmitted on said first bus from one of said first plurality of bus masters, said first mapping means also generating a SNOOP signal of a state indicating

> when a generated second address is mapped to one of said particular subset of the second data storage locations, and
>
> bus interface means connected to said first and second buses for responding to the first indicating signal when said one of said first plurality of bus masters is reading data by placing the generated second address and SNOOP signal on the second bus, receiving data from a second data storage location mapped to said second address, and transmitting the received data to said one of said first plurality of bus masters via said first bus when the said one of said first plurality of bus masters is reading data.

'369 patent col.12 l.41-col.14 l.12 (emphasis added).

II

CCCC sued Via on December 2, 2004, and Intel on April 28, 2005 for infringing the '369 patent in separate actions. The district court consolidated the actions on January 11, 2006. On October 22, 2007, the district court issued its claim construction order. On September 23, 2008, the district court granted summary judgment to Via and Intel of non-infringement of the '369 patent.

CCCC appeals the district court's claim construction and grant of summary judgment of non-infringement of the '369 patent. This court has jurisdiction under 28 U.S.C. § 1295(a).

III

This court reviews a district court's claim construction without deference. *Cybor Corp. v. Fas Techs., Inc.*, 138 F.3d 1448, 1455-56 (Fed. Cir. 1998) (en banc). Claim terms "are generally given their ordinary and customary

meaning." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal quotation marks omitted). "[T]he claims themselves provide substantial guidance as to the meaning of particular claim terms." *Id.* at 1314. In addition, a patent's specification "is always highly relevant to the claim construction analysis." *Id.* at 1315 (internal quotation marks omitted).

The claim term at issue in this case is "the SNOOP signal telling said one of said second plurality of bus masters when to write cached data to the address appearing on the bus." The district court construed this term to mean "the SNOOP signal indicating to one of the bus masters on the second bus when to write cached data to the one of the second data storage locations at the address appearing on the second bus." The district court clarified that this construction "requires the SNOOP signal to indicate to a device on the second bus that it should write data held in that device's cache memory to main memory on the second bus." The parties dispute whether the claimed SNOOP signal must tell a processor to write cached data, or whether it must merely tell the processor to determine whether it should write cached data.

The plain language of the claim states that the SNOOP signal tells the processor "when to write cached data." '369 patent col.13 ll.11-13. The abstract of the '369 patent states that "when accessing a cached memory address, the bus interface circuit places a signal on the second bus telling the second bus master to copy data from the cache memory into the main memory." *Id.* abstract. The specification also states that the processor on the second bus responds to the SNOOP signal by asserting a retry signal and writing the requested cached data back to main memory. *Id.* col.2 ll.26-35, col.12 ll.16-

24. Thus, the claim language and the patent specification support the district court's construction.

CCCC argues that the specification does not require the processor to respond to the SNOOP signal by writing cached data. Specifically, CCCC points to the following portion of the specification:

> To ensure cache coherency, when computer 4 seeks to read access a main memory 3 address, it may assert a SNOOP signal . . . . If any other device on Futurebus 12 such as computer 6 is maintaining a cache for data stored at that memory address, computer 6 may assert a "RETRY" signal which causes computer 4 to relinquish control of Futurebus 12 before completing the address cycle. At that point, computer 6 obtains control of Futurebus 12 and writes the appropriate data from cache memory 7 back into main memory 3.

Id. col.9 ll.47-57. CCCC argues that the construction of "SNOOP signal telling" cannot require writing data from cache to main memory because the computer "*may* assert a 'RETRY' signal." *See id.* col.9 ll.52-53 (emphasis added). This portion of the specification, however, does not discuss the claimed invention. It describes the prior art one-bus system in which the computer, not the interface circuit, asserts the SNOOP signal.

Accordingly, "the SNOOP signal telling said one of said second plurality of bus masters when to write cached data to the address appearing on the bus" means "the SNOOP signal indicating to one of the bus masters on the second bus when to write cached data to the one of the second data storage locations at the address appearing on the second bus." This construction requires the SNOOP signal to indicate to a device on the second bus that it

should write data held in that device's cache memory to main memory on the second bus.

IV

This court approves summary judgment when "the pleadings, depositions, answers to interrogatories, and admissions on file, together with the affidavits, if any, show that there is no genuine issue as to any material fact and that the moving party is entitled to a judgment as a matter of law." Fed. R. Civ. P. 56. This court reviews a grant of summary judgment of non-infringement without deference. *O2 Micro Int'l, Ltd. v. Monolithic Power Sys.*, 467 F.3d 1355, 1359 (Fed. Cir. 2006).

Both parties agree that none of the accused products, including the accused "snoop filter" products, generate a SNOOP signal telling a processor that it should write its cached data to a main memory address. Thus, no accused products meet the "SNOOP signal telling" limitation, and summary judgment of non-infringement was proper.

V

Accordingly, this court affirms the district court's grant of summary judgment of non-infringement of the '369 patent.

AFFIRMED